MIM/RRAM STRUCTURE WITH IMPROVED CAPACITANCE AND REDUCED LEAKAGE CURRENT

BACKGROUND

A capacitor is a passive two-terminal electrical component used to store energy electro-statically in an electric field. The forms of practical capacitors vary widely, but all contain at least two electrical conductors (electrodes) separated by a dielectric (insulator). Capacitors are widely used as parts of electrical circuits in many common electrical devices. For example, capacitors are widely used in electronic circuits for blocking direct current while allowing alternating current to pass, but can also be used to store data states, such as in a dynamic random access memory (DRAM) device.

For integrated circuits and for DRAM devices in particular, the use of metal-insulator-metal (MIM) capacitors has become widespread in recent years. These MIM capacitors are typically formed in back-end-of-line (BEOL) processing, after front-end-of line (FEOL) processing has been completed. In other words, MIM capacitors are formed in or over metal interconnect layers that extend in horizontal planes over a semiconductor substrate in which active devices have been formed. In addition to acting as capacitive elements, MIM capacitor structures are also utilized for resistive random access memory (RRAM) devices.

The present disclosure provides MIM capacitor devices, such as used in RRAM or diode devices for example, as well as methods of making and operating such devices.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** illustrates an integrated circuit device that includes an MIM capacitor structure with an improved capacitor dielectric separating upper and lower capacitor electrodes.

FIG. **2** illustrates a co-sputtering system that can be used to form the capacitor dielectrics described herein.

FIG. **3** illustrates a plot illustrating leakage current for an MIM capacitor as a function of DC bias used to sputter nano-particles on the dielectric layer.

FIG. **4** illustrates a cross-sectional view of a MIM capacitor in accordance with some embodiments.

FIG. **5** illustrates a cross-sectional view of an RRAM cell in accordance with some embodiments.

FIG. **6** illustrates a cross-sectional view of MIM diode in accordance with some embodiments.

FIG. **7-8** show examples of methods in flowchart format in accordance with some embodiments of the present disclosure.

FIGS. **9-15** depict a series of incremental manufacturing steps as a series of cross-sectional views, which are consistent with some implementations of FIG. **8**'s flowchart.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and

arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

Successive generations of MIM capacitors exhibit continually reduced or "thinned down" dielectric thicknesses, which helps provide higher density structures. However, as the capacitor dielectric of an MIM capacitor is "thinned down", the capacitance value of the MIM capacitor tends to be correspondingly reduced, which can lead to leakage current issues. For example, electrons can easily tunnel through sufficiently thin dielectric films, which can lead to excess power dissipation, circuit noise, and/or other undesired effects. To increase the dielectric constant, κ, and correspondingly increase the capacitance of MIM capacitors, this disclosure sets forth improved capacitor dielectric materials and techniques. These materials and techniques increase the capacitance of the disclosed devices while limiting current leakage between the upper and lower capacitor electrodes.

FIG. **1** illustrates a metal-insulator-metal (MIM) capacitor structure **100** included on an integrated circuit device in accordance with some embodiments. The structure **100** includes a lower metal capacitor electrode **102**, an upper metal capacitor electrode **104**, and a capacitor dielectric **106** separating the lower and upper metal capacitor electrodes **102**, **104**. To provide an increased dielectric constant, κ, the capacitor dielectric **106** is made up of an amorphous matrix made of oxide and/or nitride (oxide/nitride matrix) **108** and a plurality of metal or metal oxide/nitride nano-particles **110** that are randomly distributed over the volume of amorphous oxide/nitride matrix **108**.

In typical implementations, the amorphous oxide/nitride matrix **108** extends continuously between the upper and lower metal capacitor electrodes **102**, **104** so as to abut opposing faces **102***a*, **104***a* of upper and lower metal capacitor electrodes. Thus, although the distribution of nano-particles **110** is random in that the spacings between neighboring nano-particles can vary in a random manner from one pair of neighboring nano-particles to the next (e.g., one pair of nano-particles can be separated by a relatively small distance while the next pair of nano-particles can be spaced apart by a relatively large distance); this randomness is continuous throughout the entire volume of the amorphous oxide/nitride matrix **108** between the upper and lower capacitor electrodes **102**, **104**. Thus, aside from random